ABSTRACT

A method and apparatus for identifying potential noise failures in an integrated circuit design is described. In one embodiment, the method comprises locating a victim net and an aggressor within the integrated circuit design, modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor, and indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design.